What is claimed is:

1. A method for generating a 16-bit pseudo random number within a single clock cycle, the method comprising:

generating a first ordered sequence of eight bits on a rising edge of a clock signal, using a first linear feedback shift register (LFSR) configured to reproduce a first characteristic polynomial of degree 8;

generating a second ordered sequence of eight bits on a falling edge of the clock signal, using a second LFSR configured to reproduce a second characteristic polynomial of degree 8, where one of the first and second characteristic polynomials is irreducible; and

combining the eight bits of the first sequence and the eight bits of the second sequence to provide a 16-bit sequence.

2. The method of claim 1, further comprising choosing said first and second characteristic polynomials to be irreducible and to be distinct from each other.

3. The method of claim 1, further comprising forming said 16-bit PRN as a selected concatenation of said first sequence and said second sequence.

4. The method of claim 1, further comprising forming said 16-bit PRN as a selected interleave of said first sequence and said second sequence.

5. The method of claim 1, further comprising drawing at least one of said first and second characteristic polynomials from the set consisting of:

$p(x;8) = 1 + x^4 + x^5 + x^6 + x^8$;

$p(x;8) = 1 + x^3 + x^5 + x^7 + x^8$;

$p(x;8) = 1 + x^3 + x^5 + x^6 + x^8$;

$p(x;8) = 1 + x^2 + x^5 + x^6 + x^8$;

$p(x;8) = 1 + x^2 + x^4 + x^5 + x^6 + x^7 + x^8$;

$p(x;8) = 1 + x^2 + x^3 + x^7 + x^8$;

$p(x;8) = 1 + x^2 + x^3 + x^6 + x^8$;

$p(x;8) = 1 + x^2 + x^3 + x^5 + x^8$;

$p(x;8) = 1 + x^2 + x^3 + x^4 + x^8$;

$p(x;8) = 1 + x^2 + x^6 + x^7 + x^8$;

$p(x;8) = 1 + x + x^5 + x^6 + x^8$;

$p(x;8) = 1 + x + x^3 + x^5 + x^8$;

$p(x;8) = 1 + x + x^2 + x^7 + x^8$;

$p(x;8) = 1 + x + x^2 + x^5 + x^6 + x^7 + x^8$;

$p(x;8) = 1 + x + x^2 + x^3 + x^6 + x^7 + x^8$; and

$p(x;8) = 1 + x + x^2 + x^3 + x^4 + x^6 + x^8$.

6. A system for generating a 16-bit pseudo random number (PRN) within a single clock cycle, the system comprising:

a first linear feedback shift register (LFSR), configured to reproduce a first characteristic polynomial of degree 8 and to provide a first ordered sequence of eight bits on a rising edge of a clock signal;

a second LFSR, configured to reproduce a second characteristic polynomial of degree 8 and to provide a second ordered sequence of eight bits on a falling edge of a clock signal, where one of the first and second characteristic polynomials is irreducible; and

a circuit that receives and combines the eight bits from the first LFSR and the eight bits from the second LFSR to provide a sequence of 16 bits.

7. The system of claim 6, wherein said first and second characteristic polynomials are chosen to be irreducible and to be distinct from each other.

8. The system of claim 6, wherein said 16-bit PRN as a selected concatenation of said first sequence and said second sequence.

9. The system of claim 6, wherein said 16-bit PRN as a selected interleave of said first sequence and said second sequence.

10. The system of claim 6, wherein at least one of said first and second characteristic polynomials from the set consisting of:

$p(x;8) = 1 + x^4 + x^5 + x^6 + x^8$;

$p(x;8) = 1 + x^3 + x^5 + x^7 + x^8$;

$p(x;8) = 1 + x^3 + x^5 + x^6 + x^8$;

$p(x;8) = 1 + x^2 + x^5 + x^6 + x^8$;

$p(x;8) = 1 + x^2 + x^4 + x^5 + x^6 + x^7 + x^8$;

$p(x;8) = 1 + x^2 + x^3 + x^7 + x^8$;

$p(x;8) = 1 + x^2 + x^3 + x^6 + x^8$;

$p(x;8) = 1 + x^2 + x^3 + x^5 + x^8$;

$p(x;8) = 1 + x^2 + x^3 + x^4 + x^8$;

$p(x;8) = 1 + x^2 + x^6 + x^7 + x^8$;

$p(x;8) = 1 + x + x^5 + x^6 + x^8$;

$p(x;8) = 1 + x + x^3 + x^5 + x^8$;

$p(x;8) = 1 + x + x^2 + x^7 + x^8$;

$p(x;8) = 1 + x + x^2 + x^5 + x^6 + x^7 + x^8$;

$p(x;8) = 1 + x + x^2 + x^3 + x^6 + x^7 + x^8$; and

$p(x;8) = 1 + x + x^2 + x^3 + x^4 + x^6 + x^8$.